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14. ABSTRACT
We have achieved following goals:

- We have demonstrated the possibility to use a multiple wafer molecule beam epitaxy (MBE) system to grow 1.55 ?m InGaAs based MSM detector structure on 4" GaAs substrate.
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Final Report of 1.55 μM Sub-Micron Finger, Interdigitated MSM Photodetector Arrays with Low Dark Current

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Summary of Annual Report

We have achieved following goals:

- We have demonstrated the possibility to use a multiple wafer molecule beam epitaxy (MBE) system to grow 1.55 μm InGaAs based MSM detector structure on 4" GaAs substrate.
- Design a mask to use flip-chip approach to fabricate MSM detector. A metal solder bump inkjet system was acquired. The system has the capability to deposit 25,000 metal bumps per second. A process development is under the way to develop the technique to use this advanced system for MSM detector bonding to replace the conventional wire bonding.
- Transparent IZGO and IZO TFTs have been demonstrated, which can be integrated with MSM detectors.

I. Working with Raytheon To Demonstrate InGaAs MSM Structure Grown on 4" Lattice Mismatched GaAs Substrate

There is a strong interest in demonstrating InGaAs MSM on large diameter substrate. Currently 1.55 μm InGaAs based MSM technology is based on 2" InP substrate. In order to fabricate large array of MSM detectors, a large substrate is required. UF, has worked with the scientists in Raytheon to look in to the possible to use large area GaAs substrates for the growth of InGaAs, which is lattice matched to InP substrates.

Raytheon has the expertise on the InGaAs/InAlAs high electron mobility transistor(HEMT). The company is the world-wide leader on high speed pseudomorphic InGaAs/InAlAs HEMT, which has successfully grown InGaAs/InAlAs PHEMT on the GaAs substrates. The system used for this work can be loaded **5 of 4" GaAs substrate per growth**. The device structure is shown in Figure 1. Figure 2 shows a photograph of a 4" InGaAs MSM detector wafer.

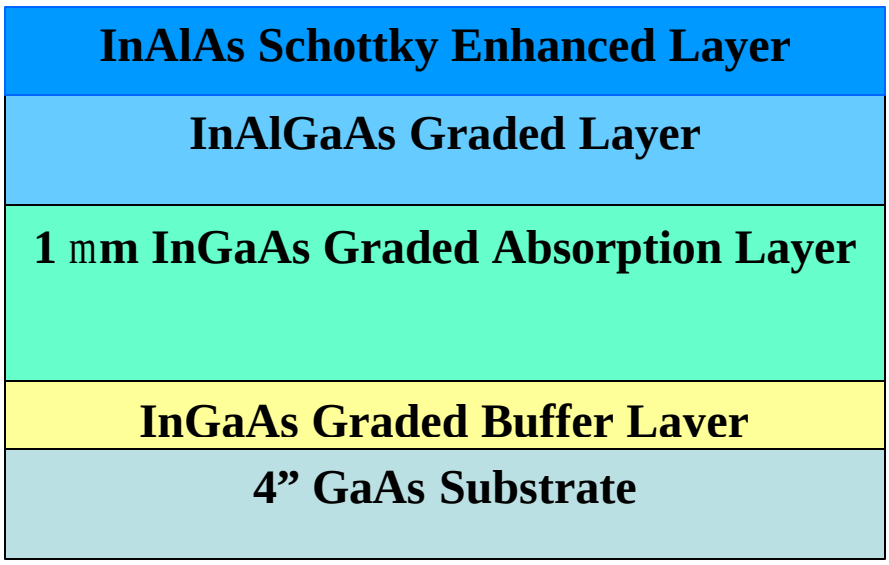


Figure 1. The layer structure of InGaAs MSM detector grown on GaAs substrate.

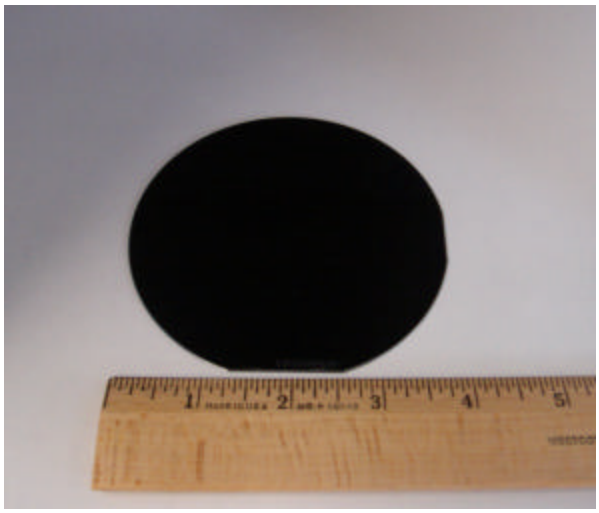


Figure 2. Photograph of a 4" InGaAs MSM detector wafer.

The different configurations of interdigitated finger based MSM detectors were fabricated on these wafer along with a 2" InGaAs MSM sample grown on InP substrate provided by Army Research Laboratories. Very similar results in terms of dark current and photo-response were obtained from these two wafers, as illustrated in Figure 3.

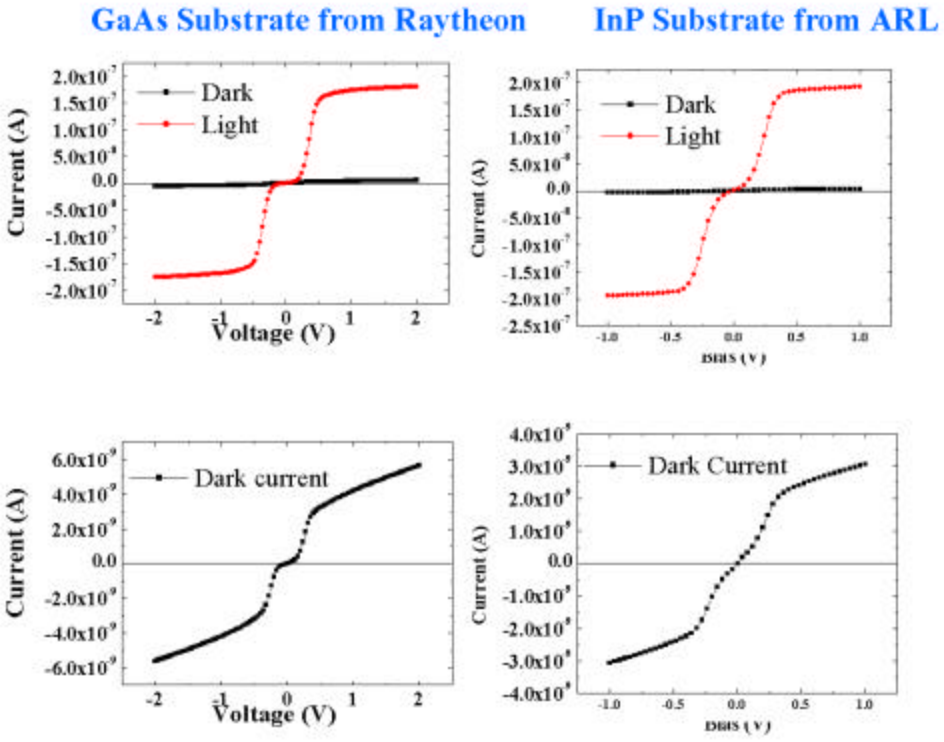


Figure 3. Dark current and photoresponse of MSM detectors fabricated on the GaAs and InP substrated.

Summary

- Demonstrated multiple-wafer large-diameter substrate growth for InGaAS MSM detectors.

II. Setting Up Metal Inkjet System for Solder Bump Deposition And Mask design

The use of ink-jet printing technology to deposit materials has been widely used in MEMS and BioMEMS devices. Ink-jet based deposition requires no tooling, is non-contact, and is data-driven: no masks or screens are required; the printing information is created directly from CAD information and stored digitally. Being data driven, it is thus flexible. As an additive process with no chemical waste, it is environmentally friendly. Ink-jet printing technology can dispense spheres of fluid with diameters of 15-200µm (2pl to 5nl) at rates of 0-25,000 per second for single droplets on-demand, and up to 1MHz for continuous droplets. Piezoelectric dispensing technology is adaptable to a wide range of material dispensing applications, such as biomedical reagents, liquid metals, and optical polymers. Although this system can be used to deposit liquids and polymers, we delicate this system to deposit metal bumps only. We acquired another Sonoplotter system for the liquid deposition.

In a continuous mode ink-jet printer, pressurized fluid is forced through an orifice, typically 50-80µm in diameter, to form a liquid jet. Surface tension acts to amplify even minute variations in the jet diameter, causing the jet to break up into drops. This behavior is normally referred to as Rayleigh breakup, because of Lord Rayleigh's observations and analysis of jet breakup in the late 1800's. If a single frequency disturbance, in the correct frequency range is applied to the jet, this disturbance will be amplified and drops of extremely repeatable size and velocity will be generated at the applied disturbance frequency. The disturbance is usually generated by an electromechanical device (e.g., a piezoelectric transducer or speaker), that creates pressure oscillations in the fluid. Figure 4 shows the operation of drop-on-demand mode.

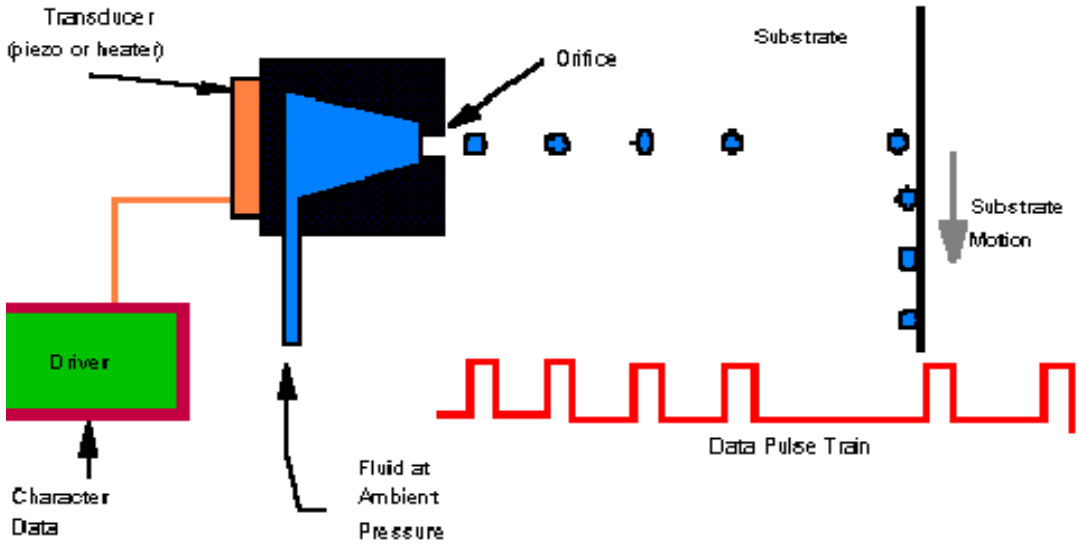


Figure 4. A schematic of drop-on-demand mode system.

Figure 5 shows the metal cartridge located on the top of a 4" wafer and some photographs of metal bumps deposited in a variety of patterns.

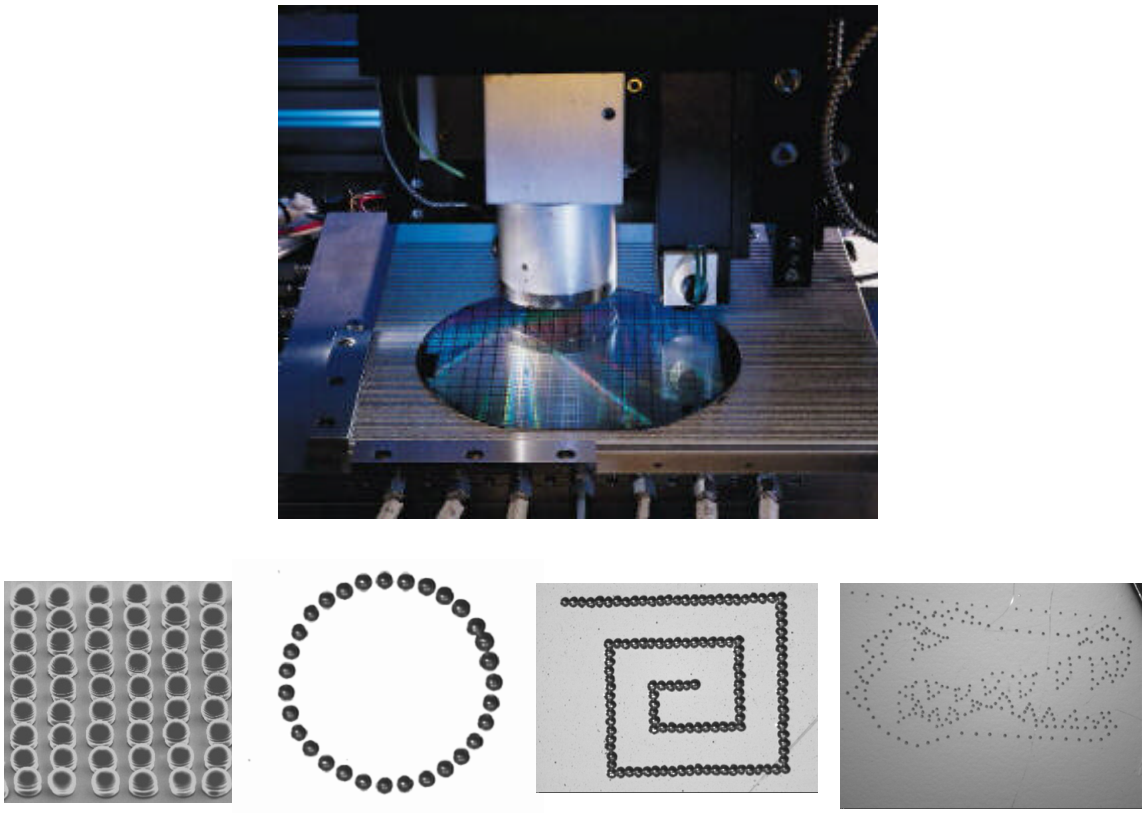


Figure 5. Photograph of a metal inkjet system is depositing metal bumps on a 4" wafer and a variety of metal bumps deposited with a drop-on-demand mode system.

A mask set of MSM detector has been designed. The detector can be package with the conventional wire bonding or use advanced flip chip bonding. Figure 6 shows the array of the detectors with conventional wire bonding approach. The majority of area are occupied by the bonding pads. For the flip chip bonding approach, the area of the MSM detector is dominated by the active area. Thus the flip chip bonding is the only way to pack the detector in high density and large array.

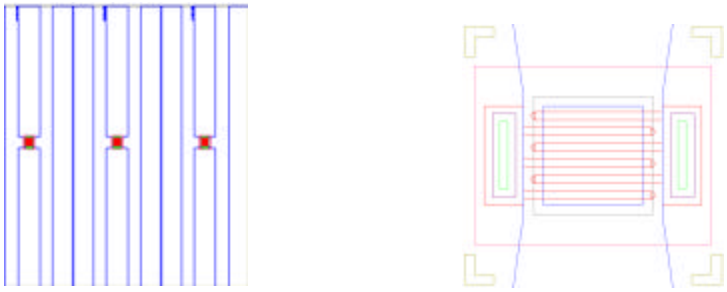


Figure 6. (right) The array of MSM detector with wire bonding approach. (left) The detector layout for the blip chip bonding approach.

III. High Performance Indium Gallium Zinc Oxide Thin Film Transistors Fabricated On Polyethylene Terephthalate Substrates

High-performance amorphous (a-) InGaZnO-based thin film transistors (TFTs) were fabricated on flexible polyethylene terephthalate (PET) substrates coated with indium oxide (In_2O_3) films. The InGaZnO films were deposited by RF magnetron sputtering with the presence of O_2 at room temperature. The *n*-type carrier concentration of InGaZnO film was ~2×10^{17} cm^{-3}. The bottom-gate-type TFTs with SiO_2 or SiN_x gate dielectric operated in enhancement-mode with good electrical characteristics: saturation mobility 11.5 $cm^2.V^{-1}.s^{-1}$ for SiO_2 and 12.1 $cm^2.V^{-1}.s^{-1}$ for SiN_x gate dielectrics and drain current on-to-off ratio $>10^5$. TFTs with SiN_x gate dielectric exhibited better performance than those with SiO_2. This is attributed to the relatively high dielectric constant (i.e. high-*k* material) of SiN_x. After more than 500 hours aging time at room temperature, the saturation mobility of the TFTs with SiO_2 gate dielectric was comparable to the as-fabricated value and the threshold voltage shift was 150 mV.

Wide bandgap oxide-based thin film transistors (TFTs) have attracted much attention for applications like flexible electronic devices. The fabrication of thin film transistors at low temperature on flexible substrates (e.g. plastic or paper) is a key technique to realize flexible electronics. So far, hydrogenated amorphous silicon (a-Si:H) [3-5] or organic semiconductor based TFTs have been widely used in display. However, they have some limitations, including light sensitivity and relatively low field effect mobilities (<1 $cm^2.V^{-1}.s^{-1}$ for a-Si:H, ~ 2.7 $cm^2.V^{-1}.s^{-1}$ for pentacene single crystals, and ~ 1.5 $cm^2.V^{-1}.s^{-1}$ for pentacene thin films). A number of groups have demonstrated TFTs based on a-oxide semiconductors such as zinc oxide (ZnO), indium gallium oxide (InGaO), zinc tin oxide (ZnSnO), indium zinc oxide (InZnO) and indium gallium zinc oxide (InGaZnO). These materials showed surprisingly high electron mobilties (~ 10 $cm^2.V^{-1}.s^{-1}$) even for a-films deposited near room temperature. High electron mobilities in the TFT channel translate to higher switching speeds of the devices. In addition, a-films have the potential for better TFT performance and stability than polycrystalline films because of the lack of grain boundaries in the channel. Amorphous-InGaZnO TFTs were first reported by Nomura et al.. The concept of transparent amorphous oxide semiconductors (TAOS) with large electron mobilities was reported earlier. However, a typical problem with the oxide-based TFTs reported in the literature has been poor device stability. Recently, we have reported that a-InGaZnO-based TFTs fabricated on glass substrates show excellent long-term stability at room temperature.

The channel was deposited on PET substrates by RF magnetron sputtering at room temperature using a 3-inch diameter $InGaZnO_4$ single target. At a deposition power of 150W, working pressure of 10 mTorr and a mixed ambient of Ar/O_2, we obtained films with carrier concentration of 2×10^{17} cm^{-3} and Hall mobility of 14 $cm^2.V^{-1}.s^{-1}$ obtained from Hall measurement. The typical thickness of InGaZnO film deposited was 50 nm, with root mean square roughness of ~ 1 nm measured over a 5×5 μm^2 area by tapping mode Atomic Force Microscopy (AFM). The film was amorphous as determined by powder x-ray diffraction (XRD), and showed optical transmittance of ~80% in the visible range. The thickness, roughness and density of the layers were identified by X-ray reflectivity (XRR). For XRR spectra, an X-ray mirror and parallel plate collimator were

used as the primary and secondary optics, respectively. The scan conditions for the sample were 0.005° step size and 3 seconds time per step.

The bottom-gate-type TFTs were fabricated using a-InGaZnO channel sputtered at room temperature and different gate dielectrics (130nm-thick SiO_2 and 80nm-thick SiN_x) deposited by PECVD at 90°C, as shown schematically in Figure 7 (top). The a-In_2O_3 and a-InZnO layers served as the TFT electrodes (gate, source and drain) which were formed by RF magnetron sputtering at room temperature. The sheet resistances of a-In_2O_3 and a-InZnO electrodes were <20O.? $^{-1}$ and ~60 O.? $^{-1}$, respectively. The TFT structure was defined using standard photolithography and lift-off processes. Photographs of the device fabricated here are also shown in Figure 7 (bottom). DC characteristics and long-term stability of the TFTs were measured using an Agilent 4156B parameter analyzer.

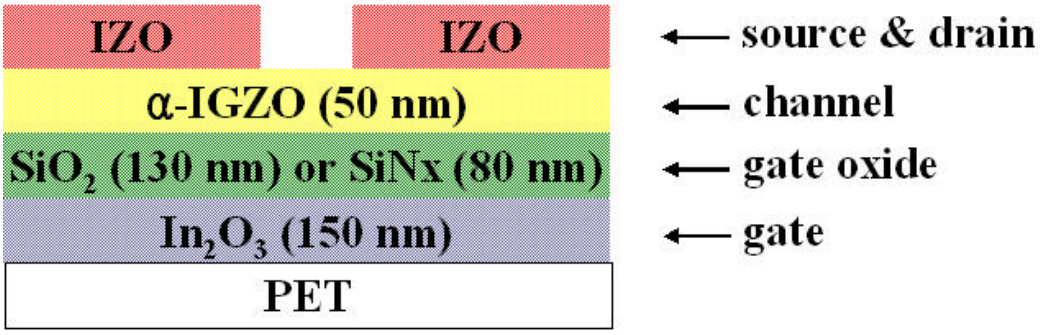


Figure 7. Schematic of a-InGaZnO thin film transistor (top) and photographs of the device (bottom).

Figure 8 shows typical output characteristics (I_{DS}-V_{DS}) for a-InGaZnO TFTs with SiO_2 (top) or SiN_x (bottom) gate dielectric. Both transistors operate in enhancement-mode with little drain current at zero gate voltage. It is also observed that the drain currents exhibit clear pinch-off voltages and current saturation, which means that the TFTs follow the standard field effect transistor characteristics. The saturation currents were ~0.023 mA for SiO_2 gate dielectric and ~0.027 mA for SiN_x gate dielectric at the bias conditions of V_{DS}=5V and V_{GS}=2.5V. The corresponding transfer characteristics at a fixed V_{DS}=5V are shown in Figure 8. There are a few observations from the I_{DS} and $(I_{DS})^{0.5}$ versus V_{GS} curves. Both TFTs showed the drain current on-to-off ratio of $>10^5$ with a low off current of $<10^{-9}$A. It demonstrates that these are promising for the

applications on high resolution flexible displays which are required to have a relatively large on-current to drive pixels and small off-current to minimize power consumption. For a-InGaZnO TFTs with SiN_x gate dielectric, the subthreshold gate-voltage swing (S) was 0.35V.decade^{-1} and given by the maximum slope in the transfer characteristic curve. The capacitance per unit area ($C_{ox,SiNx}$) of SiN_x gate dielectric was determined to be 88nF.cm$^{-2.}$ The threshold voltage (V_{th}) and saturation mobility (μ_{sat}) in the saturation region were 1.25V and 12.1 cm^2.V^{-1}.s^{-1}, respectively. This is comparable to the mobility reported for the InGaZnO TFTs fabricated on glass substrates.

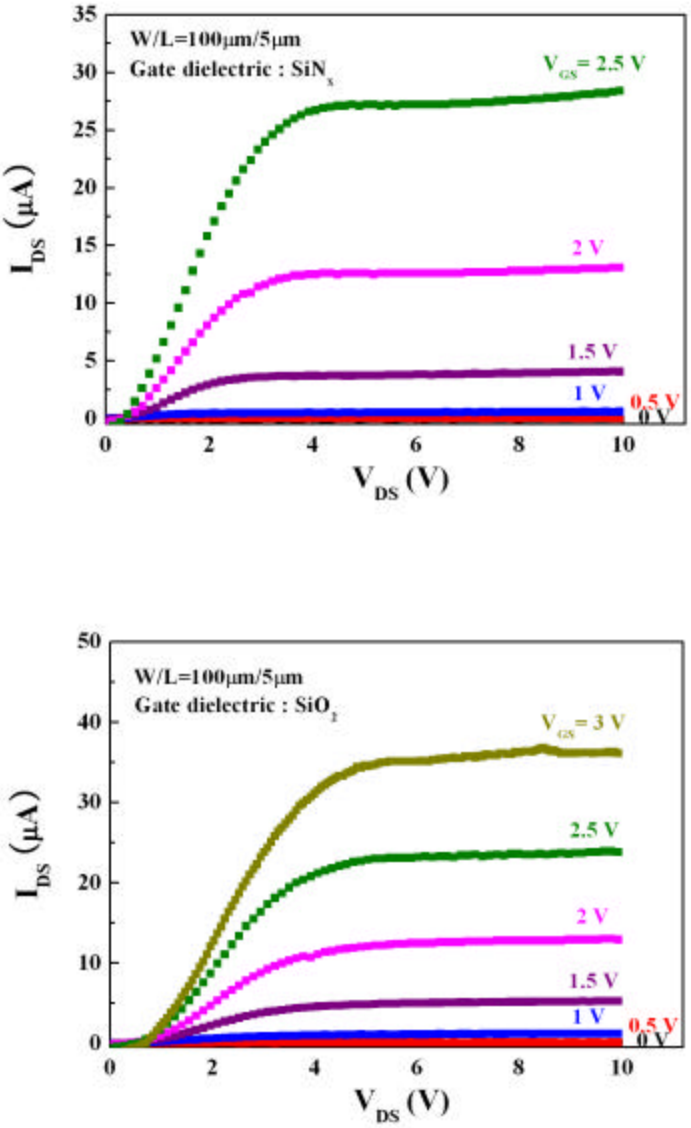


Figure 8. The typical output characteristics of a-InGaZnO TFTs with SiO_2 (top) or SiN_x (bottom) gate dielectric.

The choice of gate dielectric materials and the channel/gate dielectric interface are essential parameters which directly relate to transistor performance. The higher dielectric constant increases the transistor capacitance so that the transistor can switch properly between "on" and "off" states at low operating voltage because the high carrier density in the channel layer can be induced at a relatively low voltage range. From the transfer characteristics in Figure 9, we observed that the SiO_2 TFTs showed somewhat inferior electrical properties (μ_{sat} ~11.5 $cm^2.V^{-1}.s^{-1}$, V_{th} ~1.32V and S ~0.42V.$decade^{-1}$) to the SiN_x TFTs.

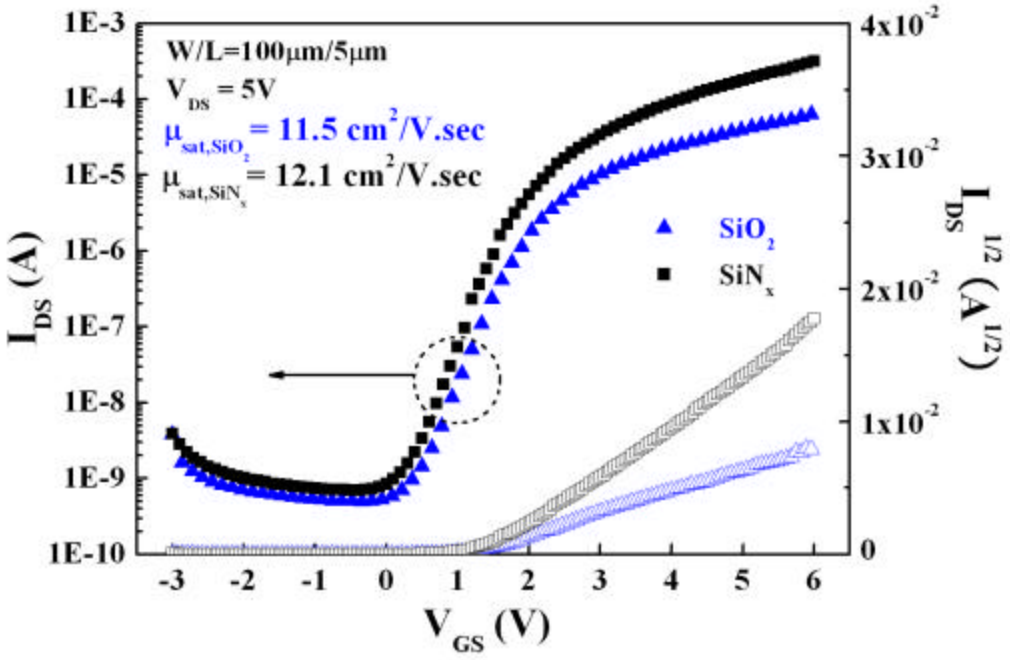


Figure 9. The transfer characteristics for a-IGZO TFTs at a fixed V_{DS}=5V.

This result is attributed to the lower dielectric constant ($e_{,SiO2}$ ~4.6 and $e_{,SiNx}$ ~8), resulting in lower capacitance ($C_{ox,SiO2}$ ~31nF.cm^{-2}) and thereby lower on-current and threshold voltage. In order to investigate the effect of interface roughness of the channel/gate dielectric on the device performance, XRR measurement was performed using multi-layer model. The interface roughnesses (2.48nm and 2.46nm, respectively) of InGaZnO-SiO_2 and InGaZnO-SiN_x were close to the surface roughness (2.27 nm) of InGaZnO film (not shown here), which can significantly reduce the scattering effect of carriers by trapped charges at the InGaZnO/gate dielectric interface. Therefore, the main influence on electrical properties of InGaZnO TFTs in this study could be the gate dielectric material.

Figure 10 (top) shows threshold voltage and saturation mobility of the TFTs with SiO_2 gate dielectric as a function of aging time at room temperature. The TFTs displayed reasonable stability at room temperature, lasting for nearly 500 hours. For our TFTs, μ_{sat} remained almost constant within experimental error during the measurement duration,

while V_{th} was slightly increased with aging time and its shift rate was 30mV/100h as also shown in Figure 10 (top and bottom). This may have been due to the bias stress during measurement, resulting in the defect state creation at channel/gate dielectric interface. The average μ_{sat} was 11.1 $cm^2.V^{-1}.s^{-1}$ and the V_{th} shift was 150mV after 500 hours aging time. In addition, the subthreshold gate voltage swing and drain current on-to-off ratio were almost unchanged at ~0.4/decade and ~10^5, respectively.

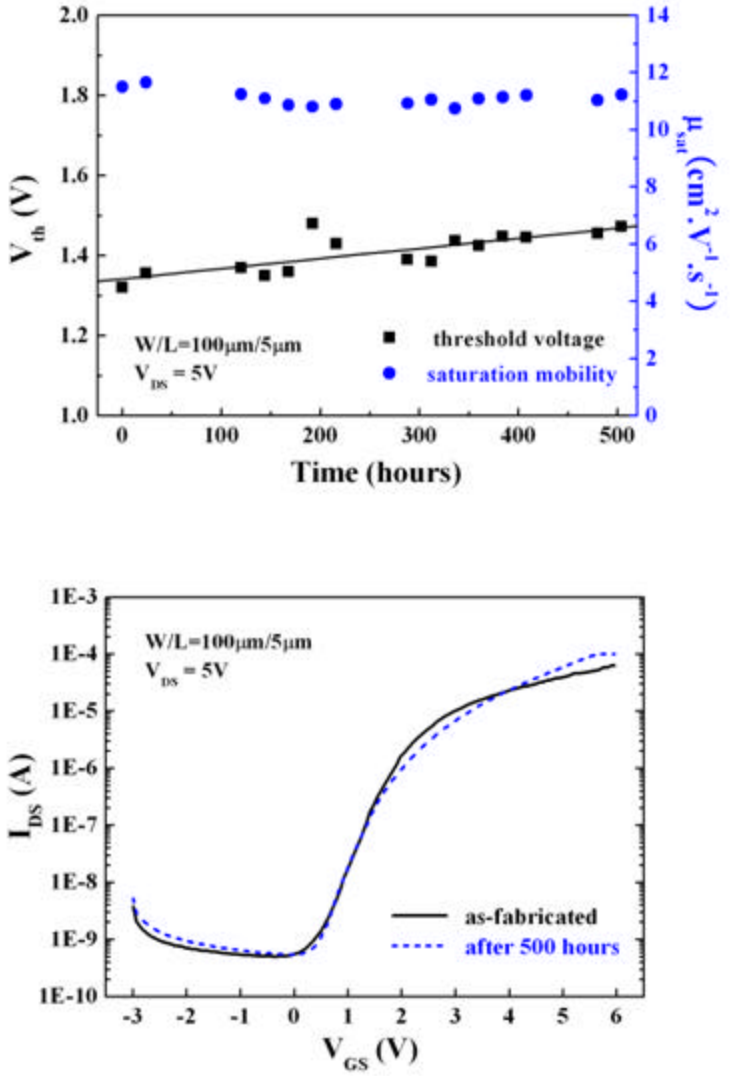


Figure 10. Change of saturation mobility and threshold voltage for a-InGaZnO TFTs with SiO_2 gate dielectric as a function of aging time at room temperature (top) and transfer characteristics after 500 aging time (bottom).

In conclusion, enhancement-mode a-InGaZnO channel TFTs with SiO_2 or SiN_x gate dielectric fabricated on flexible PET substrates exhibited high saturation mobility of >11$cm^2.V^{-1}.s^{-1}$ and high drain current on-to-off ratio of >10^5. The saturation mobility was almost constant while threshold voltage shift of the TFTs with SiO_2 gate dielectric was 150mV after more than 500 hours aging time at room temperature. a-IGZO TFTs

fabricated at low processing temperature are promising for transparent flexible electronics applications with long-term stability.

Summary

- Demonstrated a-IGZO TFTs on plastic substrates.
- Studied the effect of gate oxide on TFT performance.
- Demonstrated reliable (>500 hours) pf a-IGZO TFTs.

IV. RF Characteristics of Room Temperature Deposited Indium Zinc Oxide Thin-Film Transistors

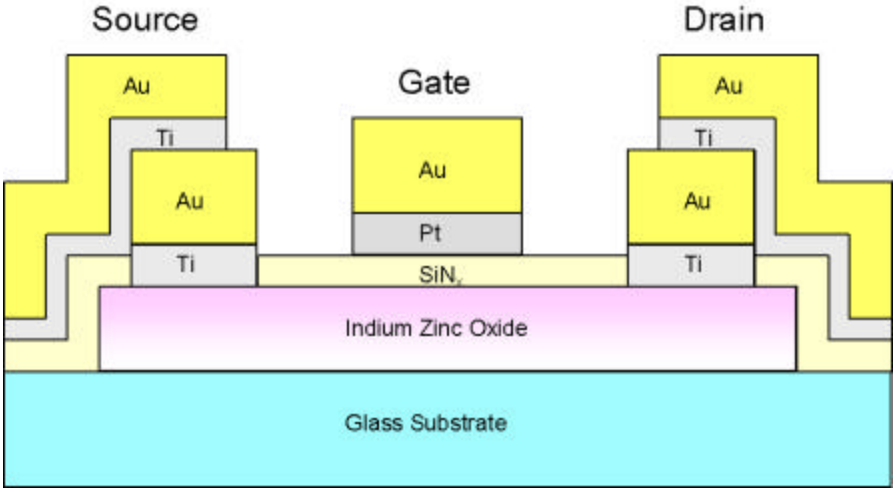
Depletion-mode indium zinc oxide (IZO) channel thin film transistors with gate dimension of 1 µm × 200 µm and drain to source distance of 2.5 µm were fabricated on glass substrates using rf magnetron sputtering deposition at room temperature. Plasma enhanced chemical vapor deposited SiN_x was used as the gate insulator. showed excellent pitch-off and the threshold voltage was around -2.5V. Saturation current density at zero gate bias voltage was 2 mA/mm and a maximum transconductance of 7.5 mS/mm was obtained at V_{ds}=3V. The drain current on-to-off ratio was $>10^5$. The maximum field effect mobility measured in the saturation region was ~14.5 $cm^2.V^{-1}.s^{-1}$. A unity current gain cut-off frequency, f_T, and maximum frequency of oscillation, f_{max} of 180 and 155 MHz, respectively, were obtained. The equivalent device parameters were extracted by fitting the measured s-parameters to obtain the intrinsic transconductance, drain resistance, drain-source resistance, transit time and gate-drain and gate-source capacitance.

There is a strong interest in developing oxide based thin film transistors due to higher transparency and better carrier mobility as compared to amorphous silicon. Amorphous or nanocrystalline n-type oxide semiconductors such as zinc oxide, zinc tin oxide, indium gallium oxide and indium gallium zinc tin oxide have shown surprisingly high carrier mobilities (~10 $cm^2\ V^{-1}\ s^{-1}$) even for amorphous films deposited at room temperature. The amorphous films are desirable over polycrystalline films because the absence of grain boundaries improves the stability and uniformity of thin film transistor (TFT) performance and the morphology is generally smoother. These transparent conducting oxides may also be used as electrodes in solar cells and flat-panel display devices. The dc characteristics of InZnO (IZO) based thin film transistors were reported previously by several groups, however, there was no report of rf performance of the IZO based TFTs.

The films were deposited on glass substrates (Corning EAGLE 2000) near room temperature by rf magnetron sputtering using 4 inch diameter targets of In_2O_3 and ZnO. The temperature at the substrate surface was ~ 40 °C after the *a*-IZO deposition, as determined from temperature indicators attached to reference glass substrates. The working pressure was varied from 2-15 mTorr in a mixed ambient of O_2/Ar.The percentage of O_2 in the mixture was varied from 0-3%. At a percentage of 2.5 %,we obtained films with carrier concentration of ~10^{18} cm^{-3} and electron mobility of 17 $cm^2.V^{-1}.s^{-1}$ obtained from Hall measurements. The partial pressure of oxygen during the sputter deposition was found to be the dominant factor controlling the conductivity of the films. The sputtering power on the targets was held constant at 125W, leading to compositions of the films measured by x-ray fluorescence spectroscopy of In/Zn=0.5 in

atomic ratio. The typical thickness of the IZO films deposited was 150 nm, with a root mean square roughness of 0.4 nm measured over a 10×10 μm^2 area by Atomic Force Microscopy. The films were amorphous as determined by x-ray diffraction and showed optical transmittance of ~80% in the visible range.

Top-gate type TFTs using 50 nm of *a*-IZO channels and 12.5 nm-thick SiN_x gate insulators deposited by plasma enhanced chemical vapor deposit ion (PECVD) were fabricated as shown schematically in Figure 11. The SiN_x layer was also deposited without heating the substrates, making the entire process consistent with typical continuous-use temperatures of commercial plastic films for electronic devices.



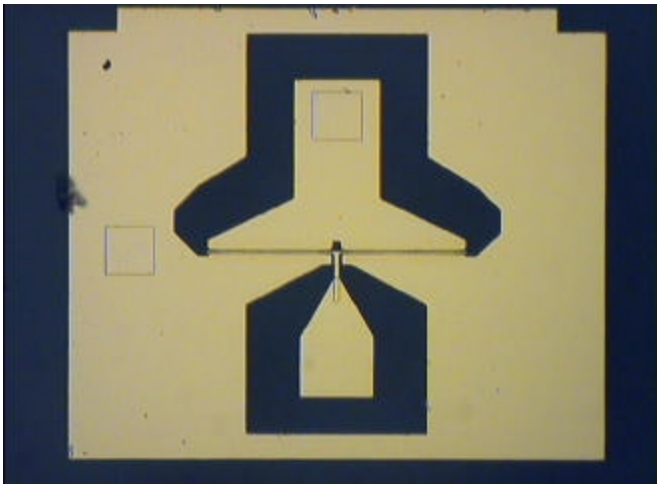


Figure 11. Schematic of an IZO transistor (top) and optical microscopy plan view of a IZO TFT(bottom).

In addition, the SiN_X gate dielectric provided superior stability of device performance relative to SiO_2 deposited under the same conditions. Figure 1 also shows a plan-view optical micrograph of a double finger TFT with a gate dimension of 1 μm × 200 μm. The gate to source and drain distance are 0.5 μm and 1.0 μm, respectively. The TFT structure was defined using photolithography and lift-off processes. The drain and source electrodes were formed with electron-beam evaporated Ti (20 nm)/Au (80 nm), which

were defined by lithography on the *a*-IZO films. The Ti/Au metallization was also used as the final metal contact. Linear transmission line patterns were also fabricated on the same substrates. Specific contact resistance and sheet resistance from the linear transmission line measurements were 7×10^{-5} O.cm^2 and 0.9 MO/sq, respectively. The dc characteristics of the transistors were obtained using an Agilent 4145B parameter analyzer and the rf measurements were conducted with an Agilent 8510 network analyzer.

Figure 12 shows typical drain current versus drain voltage, I_{DS}-V_{DS}, characteristics from the IZO transistors. The transistor operates in depletion-mode with an appreciable drain current of 2 mA/mm at zero gate voltage.

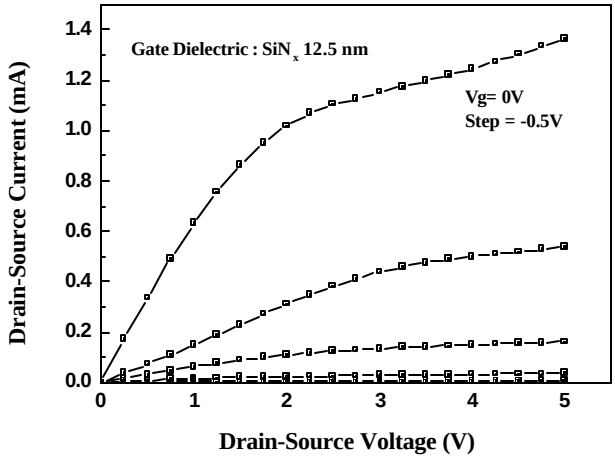


Figure 12. I_{DS}-V_{DS} characteristics of a typical IZO TFT with gate-dimension of 1 μm × 200μm.

Figure 13 shows drain current, I_{DS}, and transconductance, g_m, as a function of V_{GS} for an IZO TFT. A maximum transconductance of 7.5 mS/mm was obtained at V_{ds}=3V and V_g=0V and this is the highest transconductance ever reported for IZO based TFTs.

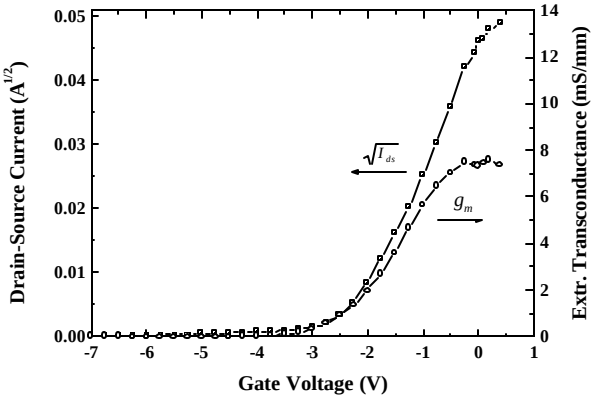


Figure 13. I_{DS} and g_m as a function of V_{GS} for a device of a typical IZO TFT measured at V_{ds}=3V.

The transistor has a threshold voltage of -2.5V, which is the gate voltage at the onset of the initial sharp increase in current in a $\log(I_D)$-V_{GS} characteristic. The field-effect mobility was extracted from the ideal metal–oxide–semiconductor field effect transistor equation in the saturation region. A value of 14.5 $cm^2.V^{-1}.s^{-1}$ was obtained, only slightly lower than the Hall mobility of ~17 $cm^2.V^{-1}.s^{-1}$ in the thicker film of the same layers. This reduced value of field mobility relative to Hall mobility is commonly observed in TFTs and suggests that there is some scattering of carriers by trapped charges at the IZO/SiN_x interface. A detailed discussion of the physical interpretations of the various types of mobilities extracted from oxide TFTs has been published previously in an IGO based TFT paper[17]. The drain and gate current are also plot in logarithmic scale verses gate voltage, as shown in Figure 14. The gate leakage current is 2×10^{-10} A and the drain current on-to-off ratio is $>10^5$.

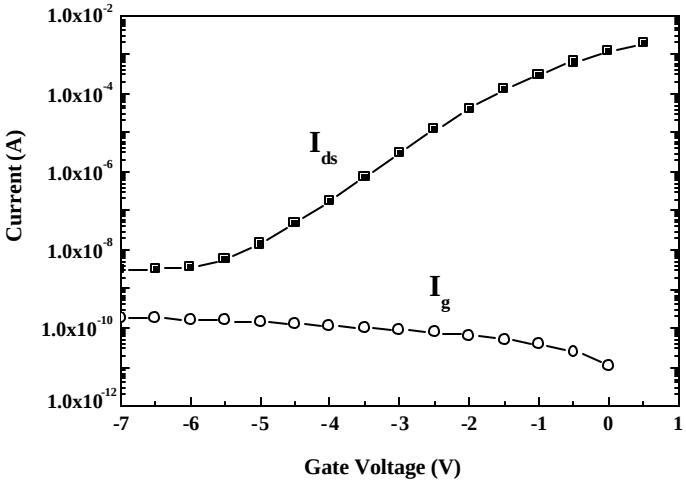


Figure 14. Drain and gate current in logarithmic scale verses gate voltage.

The TFT was biased at drain and gate voltage of 3V and 0V, respectively during the s-parameter measurements. Unity gain cut-off frequency and maximum frequency of oscillation of 180 and 155 MHz, respectively, were achieved, as illustrated in Figure 15.

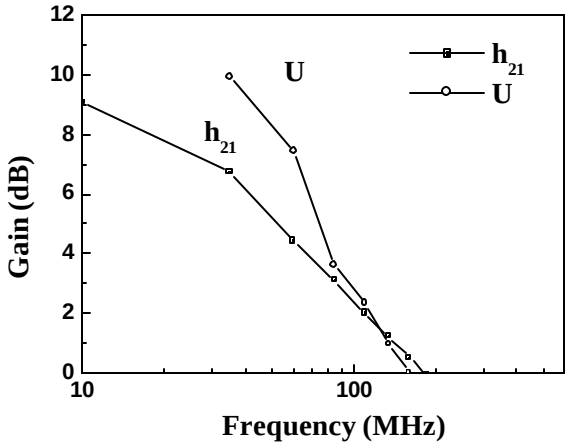


Figure 15. Calculated h_{21} and unilateral power gain of a 1 μm × 200 μm gate-dimension IZO TFT biased at V_{ds} = 3 V and V_{gs} = 0 V.

A simplified equivalent T-model for the IZO TFT, as shown in Figure 16, was used to extract the device parameters. The extracted device parameters are listed in Table I. The extracted source and drain resistance were consistent with the estimated resistance based on the transmission line measurements and drain I-V characteristics. The simulated intrinsic transconductance was very close to the measured extrinsic transconductance. The low cut-off frequency of the IZO was limited by the fairly long transit time, 16 ps, low transconductance, and high parasitic resistances, which were resulted from low mobility and saturation velocity of the α-IZO channel layer. However, this MHz range switching performance is sufficient for many display applications.

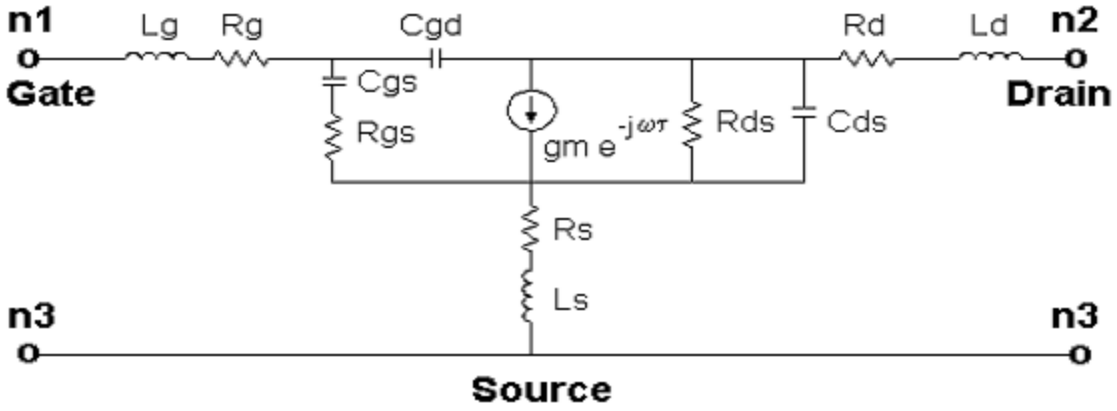


Figure 16. A simplified equivalent circuit of IZO TFT.

Table I. Extracted Device Parasitic Parameter Using A T-Model

g_m (mS)	1.4
C_{gs} (pF)	0.26
R_{ds} (Ω)	270
C_{ds} (pF)	0.01
C_{dg} (pF)	0.11
R_{gs} (Ω)	86
R_g (Ω)	17
R_s (Ω)	40
R_d (Ω)	1100
τ (pS)	16
L_g (nH)	0.01
L_s (nH)	1.7
L_d (nH)	0.03

In conclusion, dc and rf characteristics of small gate length IZO TFTs were measured. A T-model was used to extract the device parasitic parameters. This is the

first report of rf performance for IZO TFTs. The transistor showed good dc performance. An extrinsic transconductance of 7.5 mS/mm was achieved, which is the highest ever reported. The IZO thin film deposition and transistor fabrication were performed at room temperature, which makes this technology suitable for applications on organic flexible substrates.

Summary

- The first report on the rf performance of IZO FET.
- Reported the highest extrinsic transconductance of IZO TFT.

Education

- One Ph.D. student who was supported by this program graduated in May 2007.
- This program is supporting another Ph.D. candidate.
- There is no undergraduates supported by this program.

(a) Number of undergraduates funded by your agreement during this reporting period. 0
(b) Number of undergraduates funded by your agreement who graduated during this period. 0
(c) Number of undergraduates funded by your agreement who graduated during this period with a degree in a science, mathematics, engineering, or technology field. 0
(d) Number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D degree in a science, mathematics, engineering, or technology field. 0
(e) Number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense. 0
(f) Number of undergraduates graduating during this period who achieved at least a 3.5 GPA based on a scale with a maximum of a 4.0 GPA. (Convert GPAs on any other scale to be an equivalent value to a 4.0 scale.) 0
(g) Number of undergraduates working on your agreement who graduated during this period and were funded by a DoD Center of Excellence for Education, Research, or Engineering. 0
(h) Number of undergraduates funded by your agreement who graduated during this period and will receive a scholarship or fellowship for further studies in a science, mathematics, engineering or technology field. 0